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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,917	12/16/2003	Yoshihiro Koga	60188-732	3835
<div>7590 08/01/2007 Jack Q. Lever, Jr. McDERMOTT, WILL &amp; EMERY 600 Thirteenth Street, N.W. Washington, DC 20005-3096</div>			<div>EXAMINER VO, THANH DUC</div>	
			<div>ART UNIT 2189</div>	<div>PAPER NUMBER</div>
			<div>MAIL DATE 08/01/2007</div>	<div>DELIVERY MODE PAPER</div>

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

Application No.

10/735,917

Applicant(s)

KOGA ET AL.

Examiner

Thanh D. Vo

Art Unit

2189

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 June 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3, 17, 18, 20, 21, 23, 24, 26, 27, 29-31, 33, 34, 36, 37, 39, 40 and 42 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 17 and 30 is/are rejected.
- 7) ☒ Claim(s) 18, 20, 21, 23, 24, 26, 27, 29, 31, 33, 34, 36, 37, 39, 40 and 42 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## **DETAILED ACTION**

### ***Response to Amendment***

1. This Office Action is responsive to the Amendment filed on June 6, 2007. Claims 4-16, 19, 22, 25, 28, 32, 35, 38, and 41 have been canceled. Claim 1 has been amended. Claims 1-3, 17, 18, 20, 21, 23, 24, 26, 27, 29-31, 33, 34, 36, 37, 39, 40, and 42 are presented for examination. Claims 1-3, 17, 18, 20, 21, 23, 24, 26, 27, 29-31, 33, 34, 36, 37, 39, 40, and 42 are pending.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Evans et al. (US Patent 6,854,046).

As per claim 1, Evans et al. discloses a semiconductor device comprising:

a processor (Fig. 1, item 120);

a first memory unit accessed by the processor (col. 2, lines 31-32, secondary storage such as hard disk);

a plurality of page memory units obtained by partitioning a second memory unit which is different from the first memory unit and accessible by the processor at a speed higher than a speed at which the first memory unit is accessible such that each of the page memory units has a storage capacity of several kilobytes (See col. 10, lines 24-42, wherein a page is partitioned from the main memory that has a size of several kilobytes);

Evans et al. further discloses a tag (col. 14, lines 4-5) with address value (col. 2, lines 27-30) and priority information (col. 3, lines 40-42).

a tag comparator (Fig. 7) for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag (col. 2, lines 8-10); and

a replacement control unit for replacing respective contents of the page memory units. See col. 3, lines 40-48.

It is noted that Evens et al.'s invention is the improved method over the previous invention indicated at the Background of the Invention wherein the tag was used. Therefore, the invention of Evans et al. inherently comprises all of the features of a tag plus the improved method.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 2-3, 17, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans et al. (US Patent 6,854,046) in view of Yamazaki et al. (US Patent 6,233,195).

As per claim 2, Yamazaki et al. discloses a semiconductor device comprising:  
a distribution managing unit for managing the number of pages allocated to each of the page memory units for each function of an application program executed by the processor. See col. 7, lines 35-44, wherein a plurality of pages are allocated or distributed to each memory block (page memory unit). In addition, each function of an application program executed by the processor is an inherent feature in the device Yamazaki et al. since all command and/or instructions that are processed by the processor has to be executed using each of the memory block in the cache memory.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant invention to combine the method of Evans et al. with the method of Yamazaki et al. in order to arrive at the current invention. The motivation of doing so is to improve the page hit rate as disclosed by Yamazaki et al. at col. 8, lines 59-61.

As per claim 3, Yamazaki et al. discloses a semiconductor, wherein the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories (col. 8, lines 7-13), the semiconductor device further comprising:

a bank control unit for managing the plurality of bank memories is an inherent feature since the device has to have a control unit to assign a plurality of page memory into each of the bank memory.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method of Evans et al. with the method of Yamazaki et al. in order to arrive at the current invention. The motivation of doing so is to improve the page hit rate as disclosed by Yamazaki et al. at col. 9, lines 5-8.

As to claims 4, 17, and 30, Evans et al. discloses a replacement control unit determines whether or not information on a requested address is held in the tag upon receipt of an access request; select one of the plurality of page memory units if the address information is not held in the tag based on preliminarily specified replacement information; transfers data of the requested address from the first memory unit into the page memory unit. See request and replacement procedure at col. 2, lines 29-42.

***Response to Arguments***

4. Applicant's arguments filed June 6, 2007 have been fully considered but they are not persuasive.

On page 8 of the Remarks applicant indicates that Evans does not disclose or suggest that main memory 130 is partitioned into a plurality of page units, as recited in claim 1.

Applicant further argues that a page table of Evans is a data structure which stores a mapping of virtual address to physical addresses. Thus, the page table of Evans is not the same as the page units recited in claim 1. Examiner respectfully disagrees, the invention of Evans has to allocate the page table into the main memory and therefore the memory is partitioned in order to allocate such page table. The page table in the main memory of Evans inherently contains page table entries that are equivalent to the page units as recited in claim 1 of the current invention. In addition, Applicant indicates that a page table of Evans is a data structure which stores a mapping of virtual address to physical address is an irrelevant subject matter to the subject matter as being present in claim 1.

***Allowable Subject Matter***

5. Claims 18, 21, 24, 27, 31, 34, 37, and 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 20, 23, 26, 29, 33, 36, 39, and 42 are also allowable since they depending from allowable claims 18, 21, 24, 27, 31, 34, 37, and 40.

**Conclusion**

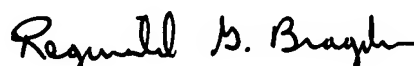
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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